IN THE CLAIMS:

Please amend the claims as set forth below.

1-30. (Cancelled)

31. (New) A processor comprising:

a register file including a plurality of registers; and

an execution core coupled to the register file, wherein the execution core, responsive to an instruction having a register address field, is configured to: (i) map a value of the register address field to a least significant portion of one of the plurality of registers responsive to the instruction including a prefix field; and (ii) map the value of the register address field to one of a least significant portion or a second least significant portion of one of a subset of the plurality of registers responsive to the instruction excluding the prefix field.

32. (New) The processor as recited in claim 31 wherein the prefix field is a prefix byte.

33. (New) The processor as recited in claim 31 wherein the instruction specifies a one byte operand size.

34. (New) The processor as recited in claim 33 wherein the least significant portion and the second least significant portion each comprise a byte.

35. (New) An apparatus comprising:

one or more storage locations corresponding to a plurality of registers; and

a processor coupled to the one or more storage locations, wherein the processor,

responsive to an instruction having a register address field, is configured to: (i) map a value of the register address field to a least significant portion of one of the plurality of registers responsive to the instruction including a prefix field; and (ii) map the value of the register address field to one of a least significant portion or a second least significant portion of one of a subset of the plurality of registers responsive to the instruction excluding the prefix field.

36. (New) The apparatus as recited in claim 35 wherein the prefix field is a prefix byte.

37. (New) The apparatus as recited in claim 35 wherein the instruction specifies a one byte operand size.

38. (New) The processor as recited in claim 37 wherein the least significant portion and the second least significant portion each comprise a byte.

39. (New) A method comprising:

mapping each value of a register address field of an instruction to a least significant portion of a different one of the plurality of registers responsive to an instruction that includes the register address field and includes a prefix field; and

mapping each value of the register address field to a least significant portion or a second least significant portion of different ones of a subset of the plurality of registers responsive to the instruction that includes the register address field and excludes the prefix field.

40. (New) The method as recited in claim 39 wherein the prefix field is a prefix byte.

41. (New) The method as recited in claim 39 wherein the instruction specifies a one byte

operand size.

42. (New) The method as recited in claim 41 wherein the least significant portion and the second least significant portion each comprise a byte.

43. (New) A computer system comprising:

a processor comprising a register file including a plurality of registers, wherein the processor, responsive to an instruction having a register address field, is configured to: (i) map a value of the register address field to a least significant portion of one of the plurality of registers responsive to the instruction including a prefix field; and (ii) map the value of the register address field to one of a least significant portion or a second least significant portion of one of a subset of the plurality of registers responsive to the instruction excluding the prefix field; and

a peripheral device configured to communicate between the computer system and another computer system.

44. (New) The computer system as recited in claim 43 wherein the prefix field is a prefix byte.

45. (New) The computer system as recited in claim 43 wherein the instruction specifies a one byte operand size.

46. (New) The computer system as recited in claim 43 wherein the least significant portion and the second least significant portion each comprise a byte.

47. (New) The computer system as recited in claim 43 wherein the peripheral device comprises a modem.

48. (New) The computer system as recited in claim 43 wherein the peripheral device comprises a network interface device.

49. (New) The computer system as recited in claim 43 further comprising a second processor comprising a register file including a plurality of registers, wherein the second processor, responsive to an instruction having a register address field, is configured to: (i) map a value of the register address field to a least significant portion of one of the plurality of registers responsive to the instruction including a prefix field; and (ii) map the value of the register address field to one of a least significant portion or a second least significant portion of one of a subset of the plurality of registers responsive to the instruction excluding the prefix field.

50. (New) The computer system as recited in claim 43 further comprising an audio device.

51. (New) A processor comprising:

a register file including a plurality of registers; and

an execution core coupled to the register file, wherein the execution core is configured, responsive to an instruction having a register address field, to: (i) utilize a first mapping of values of the register address field to the plurality of registers as a selected mapping responsive to the instruction including a prefix field; and (ii) utilize a second mapping of values of the register address field to the plurality of registers as the selected mapping responsive to the instruction excluding the prefix field, and wherein the execution core is configured to select one of the plurality of registers responsive to a value of the register address field and the selected mapping.

52. (New) The processor as recited in claim 51 wherein the first mapping maps each

value of the register address field to a least significant portion of a different one of the plurality of registers.

53. (New) The processor as recited in claim 52 wherein the second mapping maps each value of the register address field to one of a least significant portion or a second least significant portion of one of a subset of the plurality of registers.

54. (New) The processor as recited in claim 51 wherein the prefix field is a prefix byte.

55. (New) The processor as recited in claim 51 wherein the instruction specifies a one byte operand size.

56. (New) An apparatus comprising:

one or more storage locations corresponding to a plurality of registers; and

a processor coupled to the one or more storage locations, wherein the processor is configured, responsive to an instruction having a register address field, to: (i) utilize a first mapping of values of the register address field to the plurality of registers as a selected mapping responsive to the instruction including a prefix field; and (ii) utilize a second mapping of values of the register address field to the plurality of registers as the selected mapping responsive to the instruction excluding the prefix field, and wherein the processor is configured to select one of the plurality of registers responsive to a value of the register address field and the selected mapping.

57. (New) The apparatus as recited in claim 56 wherein the first mapping maps each value of the register address field to a least significant portion of a different one of the plurality of registers.

58. (New) The apparatus as recited in claim 57 wherein the second mapping maps each value of the register address field to one of a least significant portion or a second least significant portion of one of a subset of the plurality of registers.

59. (New) The apparatus as recited in claim 56 wherein the prefix field is a prefix byte.

60. (New) The apparatus as recited in claim 56 wherein the instruction specifies a one byte operand size.